Please substitute the paragraph beginning on page 46, line 20 with the following paragraph:

In the variable length decoding MBx-VLD thereof as well, the decoding is simultaneously started at the processors 2-1 to 2-3 at the start of the processing as shown in Fig. 21, therefore the second processor 2-2 and the third processor 2-3 are made to wait and the idling occurs in the processing, but, thereafter, the processing steps in the processors will always be offset from each other and such idling will hardly ever occur. Also, in the example shown in Fig. 21, no idling at all occurs in other processing – though the variable length decoding MB3-VLD of the macroblock 3 at the first processor 2-1 is made to slightly wait.

## REMARKS

Claims 1-19 are pending in the above-identified application and were rejected. Because no amendments were made to the claims, claims 1-19 remain at issue in the above-identified application.

Claims 1-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe et al. (U.S. Patent No. 5,675,331) in view of Allen et al. (U.S. Patent No. 5,583,500). Applicant respectfully traverses this rejection.

Independent claims 1 and 7 are directed to an apparatus and method, respectively, for encoding image data (e.g., according to the MPEG-2 standard). Similarly, independent claims 10 and 17 are directed to an apparatus and method, respectively, for decoding image data

(e.g., MPEG-2 coded data). The independent claims share in common that the coding (or decoding) operations are performed in parallel on multiple processing devices.

In claim 1, a first processing device includes a fixed length coding means and a variable length coding means, and a second processing device includes a fixed length coding means and a variable length coding means. Similarly, in claim 10, a first processing device includes a fixed length decoding means and a variable length decoding means, and a second processing device includes a fixed length decoding means and a variable length decoding means. In claim 7, the signal processing device that encodes a data block also carries out the variable length coding for the encoded data block. Similarly, in claim 17, each signal processing device carries out variable length decoding on an assigned data block followed by fixed length decoding of the assigned data. Accordingly, for claims 1, 7, 10, and 17, within each signal processing device, both fixed and variable length coding (or decoding) occurs.

The Examiner identified the variable-length decoder 5 of Watanabe et al. as a master processor and the fixed-length decoder 6 of Watanabe et al. as a slave processor. Thus, the Examiner equated the variable-length decoder 5 and the fixed-length decoder 6 with the signal processing devices in claims 1, 7, 10 and 17. Contrary to claims 1, 7, 10 and 17, both fixed and variable length coding (or decoding) do not occur within each of the variable-length decoder 5 and the fixed-length decoder 6 of Watanabe et al. Thus, contrary to the Examiner's conclusion, it would not have been obvious to one of ordinary skill in the art to modify the encoders of Allen into the system of Watanabe to derive claims 1, 7, 10 and 17. Accordingly, Applicant respectfully requests that the § 103 rejection of claims 1, 7, 10 and 17, and all claims dependant on claims 1, 7, 10 and 17, be withdrawn.

In view of the above remarks, Applicant submits that all claims are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

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By: _____

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## APPENDIX A
## VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE SPECIFICATION

On page 5, the paragraph starting at line 20 is amended as follows:

When the generation of headers of the different levels is ended, macroblock encoding is carried out (step S185), macroblock variable length coding is carried out (step S186), and macroblock local [encoding] decoding is carried out (step S187).

On page 5, the paragraph starting at line 25 is amended as follows:

When the encoding is ended for all macroblocks inside a slice, the processing routine shifts to the processing of the next slice (step S188). Below, similarly, when all processing of a picture is ended, the processing routine shifts to the processing of the next picture (step S189). When all processing of one GOP is ended, the processing routine shifts to the processing of the next GOP (step S190). This series of processing is repeated until the sequence is ended (step [S181),] S191), whereupon the processing is ended (step S192).

On page 23, the paragraph starting at line 10 is amended as follows:

Below, similarly, when all processings of one picture are ended, the processing routine shifts to the processing of the next picture (step S20), and when the processing of all pictures of [1GOP] one GOP are ended, the processing routine shifts to the processing of the next GOP (step S21). Then, when these processing are repeated until the sequence is ended (step S22), the processing is ended (step S23).

On page 26, the paragraph starting at line 1 is amended as follows:

Also in the third processor 2-3, similarly, when the variable length coding MB1-VLC with respect to the macroblock 1 is ended in the first processor 2-1, the local decoding [MB0-DEC] MB1-DEC with respect to that data is carried out. Then, when this local decoding [MB0-DEC] MB1-DEC is ended, the encoding MB3-ENC with respect to the next macroblock 3 is carried out.

On page 26, the paragraph starting at line 8 is amended as follows:

Below, similarly, in the first processor 2-1, the second processor 2-2, or the third processor 2-3, when the encoding MBx-ENC of the [encoding of the] macroblock to be processed next is ended, the [decoding] variable length coding MBx-VLC of the encoded data is sequentially carried out.

On page 26, the paragraph starting at line 13 is amended as follows:

Further, in the second processor 2-2 and the third processor 2-3, when the variable length coding MBx-VLC is ended in the first processor 2-1, the local [encoding] decoding MBx-DEC with respect to the macroblock thereof is carried out, and after the end of the processing, the encoding MBx-ENC with respect to the next macroblock x+1 is subsequently carried out.

On page 28, the paragraph starting at line 6 is amended as follows:

When the decoding of the slice header is ended, the master processor activates the slave processors (step S45) and carries out the variable length decoding with respect to a macroblock

(step S46). The master processor repeatedly carries out this variable length decoding (step [S4i6)] S47) until this processing is ended for all macroblocks inside the slice.

On page 46, the paragraph starting at line 20 is amended as follows:

In the variable length decoding MBx-VLD thereof as well, the decoding is simultaneously started at the processors 2-1 to 2-3 at the start of the processing as shown in Fig. 21, therefore the second processor 2-2 and the third processor 2-3 are made to wait and the idling occurs in the processing, but, thereafter, the processing steps in the processors will always be offset from each other and such idling will hardly ever occur. Also, in the example shown in Fig. [13,] 21, no idling at all occurs in other processing – though the variable length decoding MB3-VLD of the macroblock 3 at the first processor 2-1 is made to slightly wait.

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